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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/020,897 | 12/19/2001 | Jacob Midtgaard | 1076.41001X00 | 8780 |

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| EXAMINER | |
|---|---|
| RAMAKRISHNAIAH, MELUR | |
| **ART UNIT** | **PAPER NUMBER** |
| 2643 | |

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/020,897 | MIDTGAARD ET AL. | |
| | Examiner | Art Unit | |
| | Melur Ramakrishnaiah | 2643 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14 and 16* is/are allowed.

6)☐ Claim(s) *1,2,5-13,15,17-29,32 and 35-46* is/are rejected.

7)☒ Claim(s) *3,4,30,31,33 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12-19-2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5-13, 15, 17, 18-20, 22, 23, 24-29, 32, 36, 37-40, 42, 43-45, are rejected under 35 U.S.C. 103(a) as being unpatentable over Su (US PAT: 5,847,602) in view of Opas (US PAT: 5,023,937).

Regarding claims 1 and 15, Su discloses the following: an envelope loop (31, fig. 3), a phase loop (40, fig. 3) and components (for example 37, 38, 41, 42, fig. 3) disposed within each of the phase and envelope loops configured to match the transfer characteristics of the phase and envelope loops (col. 4, line 30 – col. 5, line 58).

Regarding claim 17, Su discloses the following: an envelope elimination and restoration device including a power amplifier having a bias control input (44, fig. 3), wherein the device includes an envelope detector (33/34, fig. 3) for detecting an envelope of an input signal and the output of the envelope detector is connected to the bias control input (44, fig. 3) of the amplifier to control the output of the envelope (col. 4, line 30 – col. 5, line 58, col. 6 lines 49-61).

Regarding claim 23, Su discloses the following: a device including an envelope elimination and restoration device including a power amplifier (reads on 43, fig. 3) having a bias control input (44, fig. 3) wherein the device includes an envelope detector (33/34, fig. 3) for detecting the envelope of the input signal and output of the envelope

detector is connected to the bias of control input of the amplifier to control the output signal envelope (col. 4, line 30 – col. 5, line 58, col. 6 lines 49-61).

Regarding claim 24, Su discloses envelope feedback device including a power amplifier providing an output signal, a controller (reads on 37, fig. 3) for controlling the envelope of the output signal, and a compensator (reads on 38, 39, fig. 3) for compensating for non-linear characteristics of the envelope controller (col. 4, line 30 – col. 5, line 58).

Regarding claim 36, Su discloses device including an envelope feedback including a power amplifier (43, fig. 3) providing an output signal, a controller (reads on 37, fig. 3) for controlling the envelope of the output signal, and a compensator (reads on 38, 39, fig. 3) for compensating the non-linear characteristics of the envelope controller (col. 4, line 30 – col. 5, line 58).

Regarding claims 37, 42, 43, Su discloses the following: feedback device having an arrangement for providing a difference signal representative of the difference between input and feedback signals, comprising a detector (reads on 35) configured to detect loss of feedback control to detect loss of feedback control when the difference signal exceeds a predetermined threshold (col. 5, line 55 – col. 6, line 28).

Regarding claims 5-13, 18, 19- 20, 25-29, 32, Su further teaches the following: power amplifier (43, fig. 3) for providing an output signal, wherein the envelope loop includes an envelope control system for the output signal, envelope control system includes a power supply modulator (reads on 38, fig. 3) arranged to modulate the

voltage supply of the power amplifier (col. 6 lines 49-61), envelope loop includes an envelope detector (33/34, fig. 3), envelope detector is connected to a bias control input (44, fig. 3) of the power amplifier, whereby to provide the envelope control system (col. 6 lines 49-61),compensation means (reads on 38,39, fig. 3) disposed in the envelope loop for compensation for non-linearities in the envelope control system, first and second envelope detectors (33/34, fig. 3) for detecting input and output envelops respectively and a system for providing a difference signal representative of the difference between the input and output envelopes, difference signal providing system comprises a comparator (reads on 35, fig. 3, col. 5, line 55 – col. 6, line 11), comprising a detector in (35) to detect the loss of feedback signal, detector is operative on the difference signal, a slow power supply modulator (reads on 38, fig. 3) configured to modulate the supply voltage to the power amplifier (col. 6 lines 49-61), linearising configuration includes an envelop feedback loop (32, fig. 3), power amplifier has a voltage supply and envelop controller comprises a modulator (reads on 37/38, fig. 3) for modulating the voltage supply (col. 6 lines 49-61, col. 7 lines 31-37), power amplifier (43, fig. 3) has a bias control input (44, fig. 3), the feedback further comprising a difference signal generator means (reads on 35, fig. 3) for providing a difference signal representative of the difference between input and output envelope components, wherein the difference signal is connected to the bias control input (44, fig. 3) of power amplifier (43, fig. 3) to provide envelope control means, difference signal is connected to the bias control input (44, fig. 3) of the power amplifier via loop filter (38, fig. 3), wherein difference signal generator comprises a comparator (35, fig. 3, col. 5, line 55 – col. 6,

line 11) arranged to receive signals from the first and second envelope detectors for detecting the input and output envelope components respectively, compensator (for example 39, fig. 3) is disposed between the output of the amplifier and input to the comparator(col. 4, line 30 – col. 5, line 58).

Regarding claims 38-40, 44-45, Su further teaches the following: detector comprises an amplitude detector configured to detect a loss of feedback control when the amplitude error exceeds a predetermined threshold (col. 4, line 30 – col. 5, line 58), a power amplifier (43, fig. 3) for amplifying an input signal having input phase and envelop components to produce an output signal having output phase and envelope components, an envelope loop (31, fig. 3) including elements configured to produce an envelope difference signal representative of the difference between the input and output envelope components, wherein amplitude detector is configured to monitor the difference signal, comparator (reads on 35, fig. 3) for producing the difference signal, the comparator being configured to receive output signals from the first and second envelope detectors, input and output signal components comprises signal envelope components detecting a difference signal deviation comprises detecting a difference signal amplitude greater than predefined threshold (col. 4, line 30 – col. 6, line 28).

Su differs from the claimed invention in that he does not explicitly teach the following: polar loop transmitter/portable communication device, a signal generator for generating pre-distorted signals whereby to provide linearising configuration.

However, Opas discloses transmitter with improved linear amplifier control which teaches the following: polar loop transmitter/portable communication device, a signal

generator for generating pre-distorted signals whereby to provide linearising configuration (col. 1 lines 34-51, col. 2 lines 40-42).

Thus, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify Su's system to provide for the following: polar loop transmitter/portable communication device, a signal generator for generating pre-distorted signals whereby to provide linearising configuration as this arrangement would provide for polar loop transmitter provided with a pre-distorted signals to achieve linearity of operation of the transmitter as taught Opas.

3. Claim 21 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Su in view of Opas as applied to claim 17 and 24 above, and further in view of Faulkner et al. (US PAT: 5,420,536, hereinafter Faulkner).

Regarding claims 21 and 35, the combination does not teach the following: phase feedback loop.

However, Faulkner discloses linearized power amplifier which teaches the following: phase feedback loop (fig. 1c, col. 4 lines 62-64).

Thus, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the combination to provide for the following: phase feedback loop as this arrangement would provide one of the methods, among many possible methods, to achieve linearization of the power amplifier system as shown in Faulkner, thus improving the operation of amplifier circuits.

4. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Su in view of Opas as applied to claim 37 above, and further in view of Wray et al. (US PAT: 5,467,055, hereinafter Wray).

Regarding claim 41, the combination does not teach the following: Cartesian transmitter in which the difference signal is representative of the difference between in phase I input and feedback signals or Quaternary signal Q and feedback signals.

However, Wray discloses power amplifier and radio transmitter which describes the following: Cartesian transmitter in which the difference signal is representative of the difference between in phase I input and feedback signals or Quaternary signal Q and feedback signals (col. 1 lines 24-34).

Thus, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the combination to provide for the following: Cartesian transmitter in which the difference signal is representative of the difference between in phase I input and feedback signals or Quaternary signal Q and feedback signals as this arrangement would facilitate improving the linearity of amplifier operating characteristics as taught by Wray, thus preventing the distortions of the signals which results in better performance of the device.

5. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Su in view of Opas as applied to claim 43 above, and further in view of Urayama (JP02000156796A).

Regarding claim 46, the combination does not teach the following: averaging the difference signal.

However, Urayama discloses dc component recovery device which teaches the following: averaging the difference signal (fig. 1, see abstract).

Thus, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the combination to provide for the following: averaging the difference signal as this arrangement would facilitate to eliminate signal spikes etc, thus ensuring normal values for signal processing.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Su in view of Opas as applied to claim 1 above, and further in view of Murayama (JP 403131105A).

Regarding claim 2, the combination shows the following: a loop filter (38, fig. 3 of '602) in envelope loop (31); but it does show loop filter in a phase loop.

However, Murayama discloses phase locked loop circuit which teaches the following: loop filter (3, fig. 1) in a phase loop (fig. 1, see abstract).

Thus, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the combination to provide for the following: loop filter in a phase loop as this arrangement would condition the signal to suite the application requirements as shown by Murayama.

7. Claims 3-4, 30-31, 33-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 14, 16 are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melur Ramakrishnaiah whose telephone number is (571)272-8098. The examiner can normally be reached on 9 Hr schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curt Kuntz can be reached on (571) 272-7499. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Melur Ramakrishnaiah
Primary Examiner
Art Unit 2643